CLAIMS

What is claimed is:

1. An internal voltage generation circuit, comprising:

a voltage divider for dividing a level of an internal voltage;

a comparator connected to an external voltage and the internal voltage, for comparing the divided internal voltage with a reference voltage to generate a compared output; and

a driver for supplying the external voltage to the internal voltage in response to the compared output of the comparator.

2. The internal voltage generation circuit of claim 1, wherein the voltage divider comprises resistors serially connected between the internal voltage and ground voltage.

3. The internal voltage generation circuit of claim 1, wherein the internal voltage generation circuit further comprises a reference voltage generator for generating the reference voltage having a predetermined voltage level by dividing a level of the external voltage.

4. The internal voltage generation circuit of claim 1, wherein the comparator comprises:

a first diode-type NMOS transistor the source of which is connected to

the external voltage;

a second diode-type NMOS transistor the source of which is connected to the internal voltage;

a first PMOS transistor the source and bulk of which are connected to drains of the first and second NMOS transistors, and the gate and drain of which are connected to each other;

a second PMOS transistor the source and bulk of which are connected to the drains of the first and second NMOS transistors, and the gate of which is connected to a gate of the first PMOS transistor;

third and fourth NMOS transistors connected to drains of the first and second PMOS transistors and gated to the reference voltage and the divided internal voltage, respectively; and

a fifth NMOS transistor connected between drains of the third and fourth transistors and ground voltage and gated to a signal enabling the comparator.

5. The internal voltage generation circuit of claim 4, wherein the driver is a PMOS transistor the source of which is connected to the external voltage, the gate of which is connected to the output of the comparator, the drain of which is connected to the internal voltage, and where the drains of the first and second NMOS transistors of the comparator are connected to a back bias voltage.

6. The internal voltage generation circuit of claim 4, wherein the first and second NMOS transistors are native transistors the threshold voltages of which are 0V.